

REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of October 4, 2002, and is believed to prima facie place this case in condition for allowance for the following reasons.

OK Responsive to paragraph 3 of the Official Action, proposed corrections to Figures 1A, 1B, 1C, 1D, 1E and 1F are attached hereto.

OK Responsive to paragraph 4 of the Official Action, paragraphs on page 1, 10 and 11 have been amended.

OK Responsive to paragraph 5, the paragraph extending between pages 3 and 4 has been amended to clarify the subject matter in question which is clearly illustrated in Figure 1E.

not OK Responsive to paragraph 6, claim 2 has been amended to remove process limitations, and the remaining limitations are believed to be proper structural limitations in compliance with 35 USC 112.

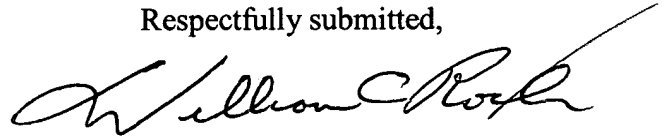
OK Responsive to paragraph 7, claims 1-5 have been reviewed in detail, and have been amended to supply proper antecedent basis for all of the terms therein, and the Examiner is thanked for pointing out those inconsistencies.

Claim 1 has also been amended on line 4 to more clearly cover the ^{only one side of the trench} embodiments discussed at page 3, wherein straps are formed on both sides of the trench, on more than a single sidewall of the trench).

In addition to the foregoing, pursuant to the requirements, applicants also enclose a "Version with Markings Showing Changes Made" to facilitate the Examiner's review of the present amendment.

The indication of allowable subject matter in paragraph 8 is noted with appreciation, and accordingly this application is now believed to be prima facie in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "William C. Roch", with a long, sweeping horizontal line extending from the end of the signature.

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WCR/sf

Enclosures Version with Markings

“VERSION WITH MARKINGS SHOWING CHANGES MADE”

IN THE SPECIFICATION:

The paragraph on page 1, lines 17-28, has been amended as follows.

A processing scheme employed in forming the above-described vertical DRAM cell arrays is described in detail in commonly-owned, co-pending U.S. Patent Application No.

09/777,576 entitled STRUCTURE AND METHOD FOR A COMPACT TRENCH-

CAPACITOR DRAM CELL WITH BODY CONTACT (~~FIS920000326, Atty Dekt #13938~~)

the contents and disclosure of which are incorporated by reference as if fully set forth herein.

Described now with reference to Figures 1(a)- 1(f) are the various processing steps for forming vertical DRAM cell arrays. As shown in Figure 1(a), there is depicted an initial structure that is employed in fabricating a vertical DRAM cell array. Specifically, Figure 1(a) shows an array portion of the structure that includes Si-containing substrate 10 having a material stack comprising an etch stop pad layer 12 and a hard mask 14 formed thereon. The substrate may include well regions 11, or the well regions may be formed later in the process.

The paragraph extending between pages 3 and 4 has been amended as follows.

An OSS process is then performed which may include the following processing steps: removing a portion of the polysilicon placeholder material using an etch process that is selective to the etch stop liner on a side of the deep trench where a strap is to be formed; removing the exposed collar oxide by utilizing an isotropic oxide etching process; removing portions of the etch stop liner and the node dielectric that are not protected by the remaining

region of the polysilicon placeholder material; removing the remaining polysilicon placeholder material; opening a portion of the oxide layer over the deep trench polysilicon not covered by the etch stop liner; continuing the oxide etching so as to form a divot in the top collar oxide at approximately the top level of the deep trench conductor; and filling the divot with a conductive material such as doped polysilicon so as to provide a bridge between the deep trench conductor and the wall of the trench. During a subsequent annealing step, dopant from the divot filled region diffuses forming buried-strap outdiffusion region 24. The divot filled ~~collar oxide~~ region is labeled as 26 in the drawings. Note that on the remaining wall portion of the structure not containing buried-strap outdiffusion 24 and divot filled ~~collar oxide~~ region 26 is an "intact" collar oxide region 18, both directly beneath the divot filled region 26 and also on the wall not having a strap which extends all the way to the etch stop pad layer 12. The intact collar oxide serves to electrically isolate body region 19 from trench capacitor 22.

The three paragraphs on page 10, lines 4-26, have been amended as follows.

After growing the gate oxide 70, the gate conductor polysilicon (or α -Si) deposited as described herein with respect to Figure 1(f). Figure 2(f) illustrates removal of the excess gate poly and the TTO HDP oxide 28 on the top of the pad nitride 14 down to the level of the pad nitride. The gate poly 70 and the TTO HDP 28 on the pad nitride 14 are removed by any of the techniques discussed in commonly-owned, co-pending United States Patent Application Serial No. 09/675,435, entitled AN EXTENDIBLE PROCESS FOR IMPROVED TOP OXIDE LAYER FOR DRAM ARRAY AND THE GATE INTERCONNECTS WHILE PROVIDING SELF-ALIGNED GATE CONTACTS

(~~Att'y Dekt. No. FIS920000342US1~~) the whole contents and disclosure of which is incorporated by reference as if fully set forth herein.

Figure 2(g) illustrates the next step of removing the pad nitride 14 by stripping it away selective to the gate poly 12 leaving poly pillars 80 extending above the silicon surface, as discussed in co-pending United States Patent Application Serial No. 09/675,435 (~~Att'y Dekt. No. FIS920000342US1~~). An optional Contact to Bitline (CB) etch-stop liner may also be deposited on the substrate surface at this stage in the process. This liner could be selectively removed from the tops of the poly-Si after the top oxide is deposited and planarized down to expose only these top surfaces.

Figure 2(h) illustrates that finally the HDP oxide 90 is deposited over the poly pillars, and the top oxide HDP is removed (e.g. polished) down to the tops of the poly pillars, as discussed in co-pending United States Patent Application Serial No. 09/675,435 (~~Att'y Dekt. No. FIS920000342US1~~).

The paragraph on page 11, lines 9-11, has been amended as follows.

Nitride liner is easily removed from the top surface when combined with method disclosed in co-pending United States Patent Application Serial No. 09/675,435 (~~Att'y Dekt. No. FIS920000342US1~~) to avoid complications with CB etch.

IN THE CLAIMS:

1. (Amended) A DRAM cell array which comprises:

a plurality of memory cells which are arranged in rows and columns, each memory cell including a deep trench region having a vertical MOSFET and an underlying capacitor formed

therein that are in electrical contact to each other through at least one a buried-strap outdiffusion region which is present within a portion of a wall of each deep trench; and,

each memory cell having a deep trench conductor forming an electrode of said underlying capacitor and ~~an oxide~~ a collar oxide region formed in a portion of the deep trench;

the collar oxide region formed on a remaining wall portion of ~~the structure~~ each deep trench not containing said buried-strap outdiffusion region for electrically isolating a body contact from said underlying capacitor; and

a trench top oxide (TTO) layer formed on a horizontal surface of the ~~structure~~ DRAM cell array for isolating ~~a~~ the deep trench conductor forming an electrode of said underlying capacitor and said buried-strap outdiffusion region from a gate conductor region;

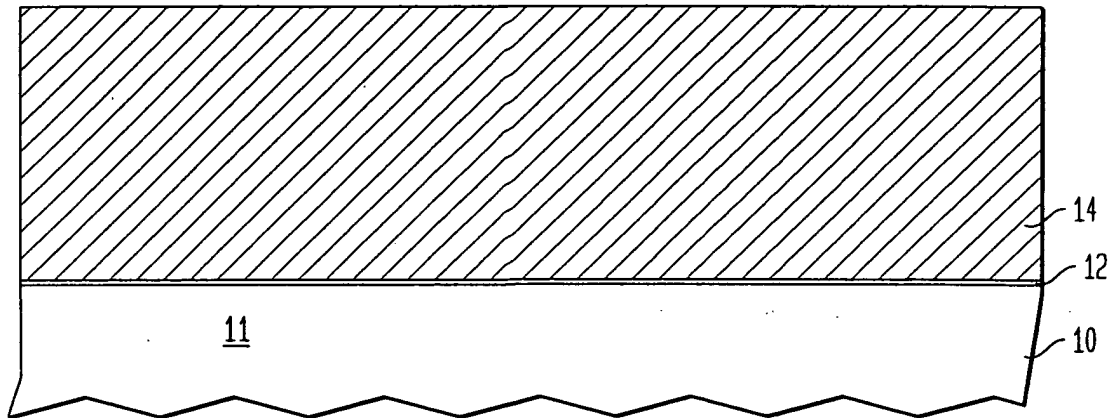
an underlying nitride layer formed between a top of said deep trench conductor and said buried-strap outdiffusion region and underlying said ~~formed~~ TTO layer to eliminate a possibility of TTO layer dielectric breakdown between said gate conductor region and said ~~capacitor~~ electrode of said underlying capacitor.

2. (Amended) The DRAM cell array of Claim 1, wherein said TTO layer is additionally formed on sidewalls of the DRAM cell array and said horizontal surface, ~~said memory cell~~ being subject to a TTO oxide sidewall etch for removing said deposited TTO from said sidewall, wherein said underlying nitride layer is additionally formed to line said sidewalls sidewall regions to protect said collar oxide region and prevent said buried-strap outdiffusion region from being etched during ~~said~~ a TTO oxide sidewall etch process.

3. (Amended) The DRAM cell array of Claim 1, further including a sacrificial oxide layer formed underneath said nitride layer ~~formed~~ to further eliminate a possibility of TTO layer dielectric breakdown between the gate conductor region and said deep trench conductor.
4. (Amended) The DRAM cell array of Claim 1, wherein said nitride ~~liner~~ layer is deposited to a thickness ranging from 1.0 nm – 10.0 nm.
5. (Amended) The DRAM cell array of Claim 1, wherein each said vertical MOSFETs ~~include~~ MOSFET includes gate dielectrics formed on inner surfaces of said sidewalls ~~walls~~ of each said ~~memory cell~~ deep trench.



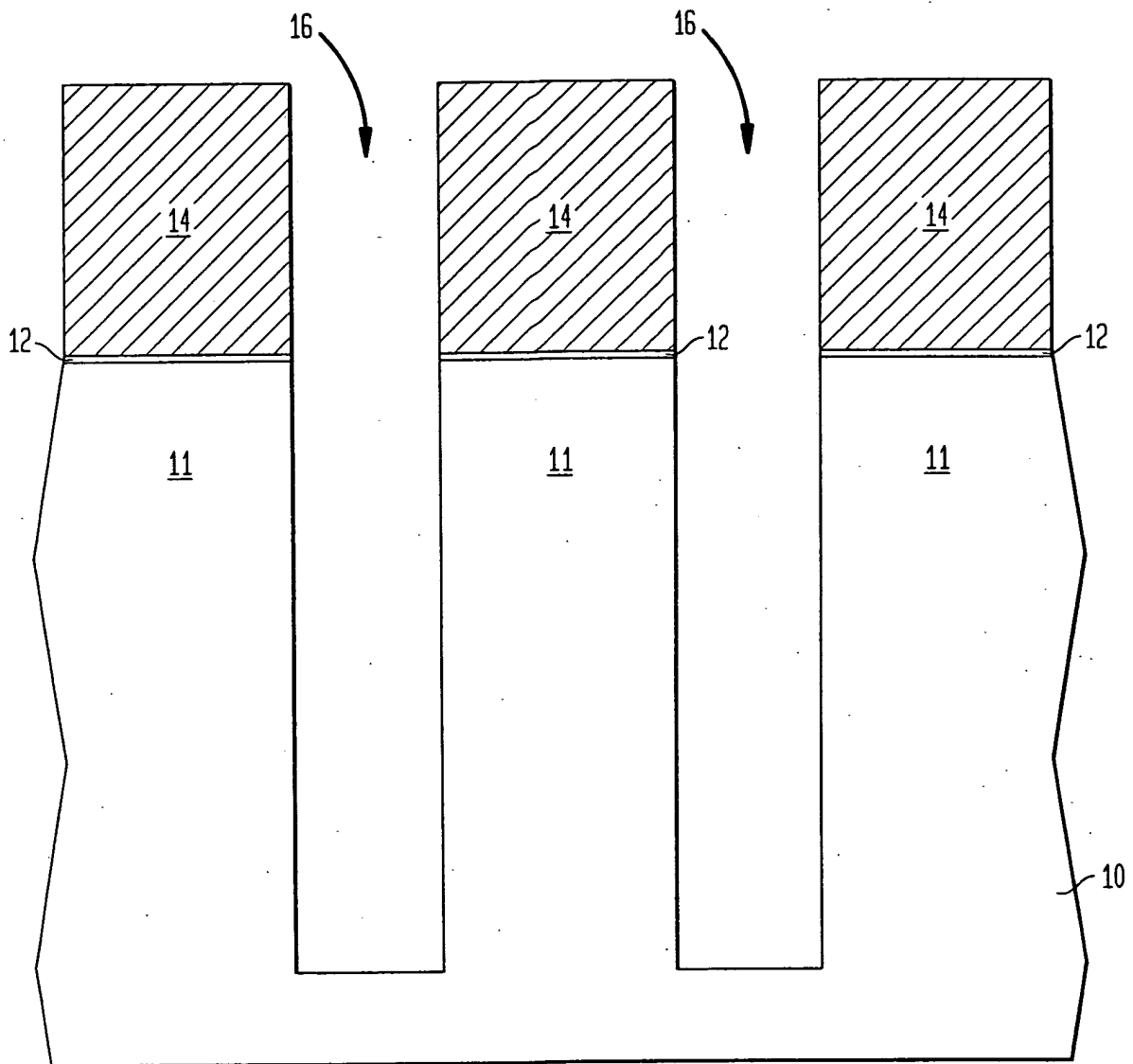
FIG. 1A (PRIOR ART)



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FIG. 1B (PRIOR ART)



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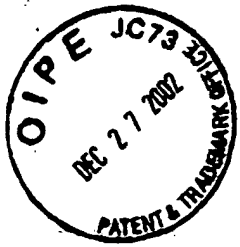
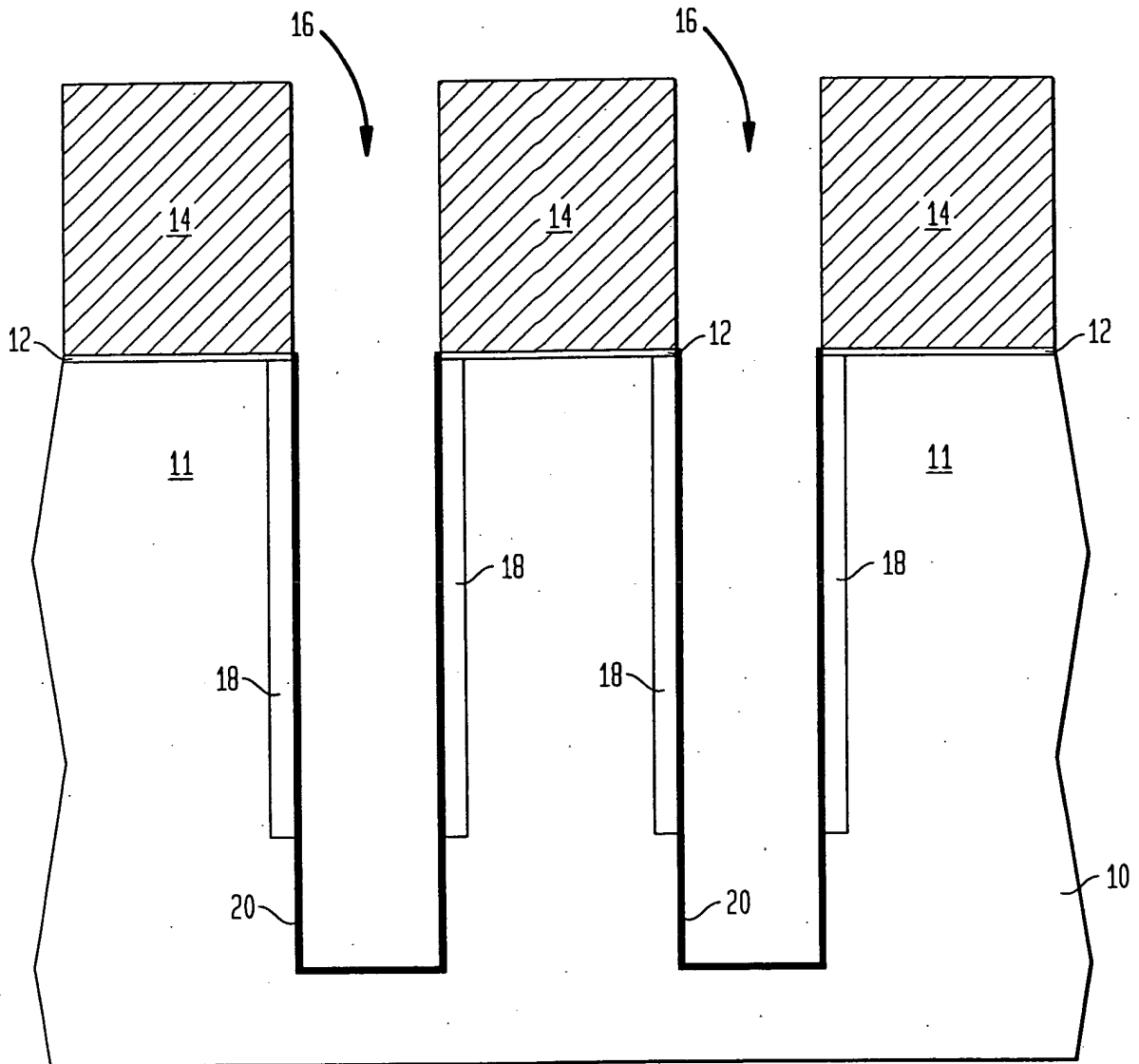


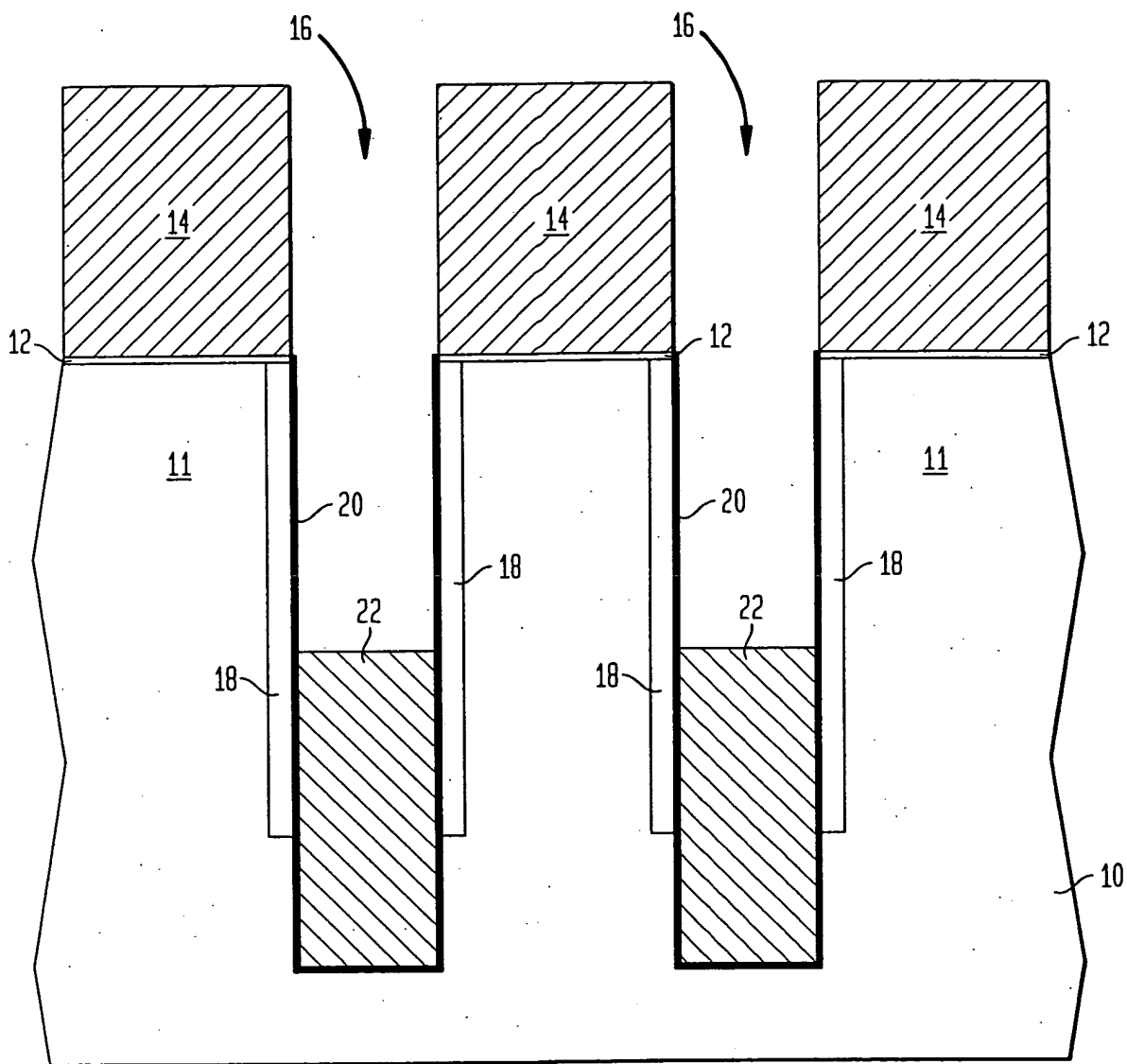
FIG. 1C (PRIOR ART)



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FIG. 1D (PRIOR ART)

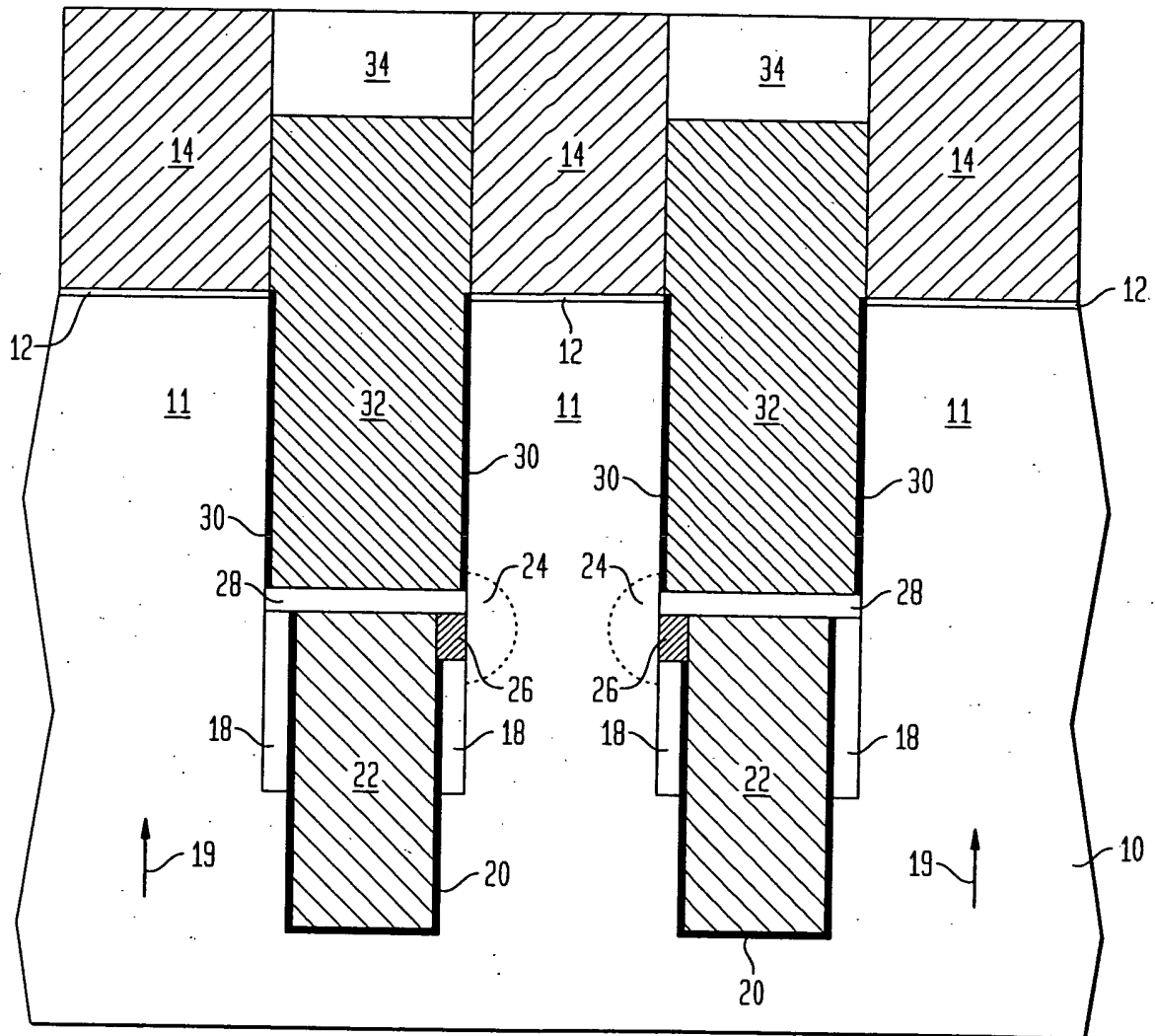


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FIG. 1F (PRIOR ART)



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